

## FACSIMILE

Page 3

## PROPOSED AMENDMENTS TO THE SPECIFICATION

Replace the two paragraphs beginning on page 3, line 24 of the specification as originally filed with the following three paragraphs:

Figure 7 is a schematic illustration of a pseudo-static memory architecture according to a third aspect of the present invention; [[and]]

Figure 8 is a timing diagram showing parallel read and refresh operations according to a sixth embodiment of the present invention[.]; and

Figure 9 illustrates the row addresses stored in each sub-array according to an addressing example.

Insert the following paragraph after line 22 on page 9:

Figure 9 illustrates the row addresses stored in each of the first, second, third, and fourth sub-arrays according to the above addressing example. The figure shows an expansion of the row addresses in each sub-array per the addressing example. Thus, the figure shows an expansion of addresses of the form XXX00XXXXXXXX stored in the first sub-array. Likewise, the figure shows an expansion of addresses of the form XXX01XXXXXXXX stored in the second sub-array. Similarly, the figure shows an expansion of addresses of the form XXX10XXXXXXXX stored in the third sub-array. Finally, the figure the figure shows an expansion of addresses of the form XXX11XXXXXXXX stored in the fourth sub-array.